REMARKS

Claims 19-37 are all the claims pending in the application. Claim 37 has been newly added herewith.

Claim Objections

Claim 19 stands objected to because of an informality. Applicants have amended claim 19 in a manner believed to overcome the objection.

Claim Rejections - 35 U.S.C. § 102

Claims 19-36 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Horst et al. (U.S. Patent No. 5,751,932). Applicants respectfully traverse.

Claim 19 recites that data is written to the first memory of the first computer module and that the same data is written to the second memory. For example, a non-limiting embodiment of the specification teaches that data is written to memory 111 by processor 101 and that the same data is written in memory 112 by processor 103 (*see* Fig. 4 and page 11, line 16 to page 12, line 14). Claim 19 also recites that during a rejoining process, the first processor switches from working by means of said first memory which is on the first computer module to working by means of said second memory which is on the same computer module. Claim 19 is allowable at least because Horst does not disclose either that the same data is written to a first and second memory or the claimed switching as set forth in claim 19.

The Examiner asserts that Horst memory 28 constitutes both first and second memories. Particularly, the Examiner asserts that one half (*i.e.*, an upper 32-bits of data) of memory 28

constitutes a first memory and another half (*i.e.*, a lower 32-bits of data) of memory 28 constitute a second memory.[1] However, even if the upper 32-bits of data and the lower 32-bits are considered first and second memories, the same data would not be written to each of these memories, as claimed. The upper 32-bits (first memory) and lower 32-bits (second memory) are merely parts of a whole 64-bit data. Particularly, Horst teaches a system having a 64-bit address /data bus (column 14, line 25) and R4000 type processors (column 14, line 29) which are capable of using the 64-bit address. In this type of system, the same data is not written to each of the 32-bit halves of a 64-bit whole. Therefore, Horst is deficient with respect to claim 19 at least because it does not teach the same data being written to a first and second memory as claimed.

Horst is also deficient at least because if fails to teach processors switching from working by means of said first memory which is on the same computer module to working by means of said second memory which is on the same computer module. In Horst, the processor reads the 64-bit data (the upper 32-bits and the lower 32-bits/first and second memories) as a unit. Thus, the processor either reads or works by means of both the first and second memories or it does not. Horst does not switch from a state in which it switches from working by means of the first memory (upper 32-bits) to working by means of the second memory (lower 32-bits). Indeed,

[1] Applicants note that the Examiner does not specify whether the upper 32-bits are considered the first memory and the lower 32-bits are considered the second memory or vice versa. For the sake of convenience, Applicants refer to the upper 32-bits as the alleged first memory and the lower 32-bits as the alleged second memory, but reversing the characterization would not effect the substance of Applicants' comments.

since the upper and lower 32-bits are both part of a whole 64-bits, it would be meaningless to use one without the other.

In view of the above, claim 19 is allowable at least because Horst fails to teach that the same data is written to both the first and second memories and because Horst fails to teach switching from working by means of a first memory to working by means of a second memory. Claims 20-36 are allowable at least by virtue of their dependency from claim 19.

New Claim

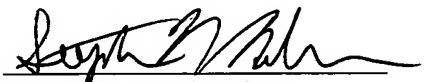
Applicants have added new claim 37 in order to provide a more varied scope of protection. Claim 37 recites that the "first processor writes data to said first memory and said second processor writes said data to said second memory." Therefore, the same data is written to both the first and second memories. Claim 37 also recites that "said first processor switches from reading said data from said first memory in a first state to reading said data from said second memory in a second state." Claim 37 is allowable at least because Horst does not disclose these features.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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